

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Fabrication method for a semiconductor structure having a partly filled trench, having the following steps:
 - (a) provision of a semiconductor structure having a trench;
 - (b) filling of the trench with a filling in such a way that the filling projects above a surface of the semiconductor structure by a first height, the filling covering the trench and the periphery of the trench;
 - (c) planarization of the filling in a first etching step in such a way that the filling is essentially planar with the surface of the semiconductor structure; [[and]]
 - (d) sinking of the filling in the trench in a second etching step by a predetermined depth proceeding from the surface of the semiconductor structure;
 - (e) essentially the same plasma power and the same etchant composition being used for the first and second etching steps; and
 - (f) wherein a planarization of the filling is carried out in a zeroth etching step before the first etching step in such a way that the filling projects above the surface of the semiconductor structure by a second height, the filling covering the trench and the periphery of the trench, the zeroth etching step having a higher etching rate than the first etching step.
2. (Canceled)

3. (Previously Presented) Method according to claim 2, wherein essentially the same etchant composition as for the first and second etching steps but an increased plasma power are used for the zeroth etching step.
4. (Previously Presented) Method according to claim 1, wherein at least the first etching step is carried out with a first time duration which is determined by an end point identification.
5. (Previously Presented) Method according to claim 2, wherein the zeroth etching step and the second etching step are carried out with a predetermined zeroth and second time duration.
6. (Previously Presented) Method according to claim 1, wherein the second etching step is carried out with a second time duration which is determined by an end point identification.
7. (Canceled)
8. (Previously Presented) Method according to claim 1, wherein the semiconductor structure comprises a semiconductor substrate and a mask situated thereon, the mask being used for the etching of the trench.
9. (Currently Amended) Method according to claim ~~[[1]]~~ 4, wherein the end point identification is carried out by interferometry.
10. (New) Fabrication method for a semiconductor structure having a partly filled trench, having the following steps:
 - (a) provision of a semiconductor structure having a trench;

- (b) filling of the trench with a filling in such a way that the filling projects above a surface of the semiconductor structure by a first height, the filling covering the trench and the periphery of the trench;
- (c) planarization of the filling in a first etching step in such a way that the filling is essentially planar with the surface of the semiconductor structure;
- (d) sinking of the filling in the trench in a second etching step by a predetermined depth proceeding from the surface of the semiconductor structure;
- (e) essentially the same plasma power and the same etchant composition being used for the first and second etching steps; and
- (f) wherein the etchant composition contains SF_6 , Ar and Cl_2 .